ABSTRACT OF THE DISCLOSURE

Provided is a TLB that can translate rapidly a virtual address to a physical address at small power consumption. A tag entry part (808) includes an ASID hold part (810), virtual address hold part (811), valid bit part (812), ASID comparison judgment part (102), and a virtual address comparison judgment part (104). By an ASID match line (105), a plurality of CAM cells (813) of the ASID hold part (810) are connected in parallel to each other and also connected to the ASID comparison judgment part (102). By a virtual address match line (106), a plurality of CAM cells (813) of the virtual address hold part (811) are connected in parallel to each other and also connected to the virtual address comparison judgment part (104). An ASID effective signal (107) is provided from the ASID comparison judgment part (102) to the virtual address comparison judgment part (104).